

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
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**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,572,710	November 5, 1996	Asano et al.			
	5,606,698	February 25, 1997	Powell			
	6,975,138	December 13, 2005	Pani et al.			
	7,382,156	June 3, 2008	Pani et al.			

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	3-961028	August 15, 2007	Japan			Abstract	
	2001-510650	July 31, 2001	Japan			Abstract only	
	2002-0033457	January 31, 2002	Japan			Abstract	

**OTHER DOCUMENTS**

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Becker, J., "A Partitioning Compiler for Computers with Xputer-based Accelerators," 1997, Kaiserslautern University, 326 pp.
	Hartenstein et al., "Parallelizing Compilation for a Novel Data-Parallel Architecture," 1995, PCAT-94, Parallel Computing: Technology and Practice, 13 pp.
	Hartenstein et al., "A Two-Level Co-Design Framework for Xputer-based Data-driven Reconfigurable Accelerators," 1997, Proceedings of the Thirtieth Annual Hawaii International Conference on System Sciences, 10 pp.
	Huang, Libo et al., "A New Architecture for Multiple-Precision Floating-Point Multiply-Add Fused Unit Design," School of Computer National University of Defense Technology, China, IEEE 2007, 8 pages.
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	XILINX, White Paper 370: (Virtex-6 and Spartan-6 FPGA Families) "Reducing Switching Power with Intelligent Clock Gating," Frederic Rivoallon, May 3, 2010, pp. 1-5.
	XILINX, White Paper 298: (Spartan-6 and Virtex-6 Devices) "Power Consumption at 40 and 50 nm," Matt Klein, April 13, 2009, pp. 1-21.
EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	